AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): A memory cell comprising:

a variable resistor; and

a current controlling device for controlling a current flowing through said variable resistor,

wherein said current controlling device is controlled by a bit line, a word line, and a source drive line,

wherein said bit line is connected to a column address signal unit of a column decoder, said column address signal unit comprises

said word line connected to a row decoder for selecting said word line,

said bit line connected to said column decoder for selecting said bit line,

and a readout circuit connected to said column decoder to read memory data from said memory cell.

Claim 2 (original): A memory cell in accordance with claim 1, wherein said current controlling device is a field-effect transistor.

Claim 3 (original): A memory cell in accordance with claim 1, wherein said current controlling device is a diode.

Claim 4 (original): A memory cell in accordance with claim 1, wherein said current

controlling device is a bipolar transistor.

Claim 5 (original): A memory cell in accordance with claim 2, wherein said variable resistor has a resistance body of a perovskite structure.

Claim 6 (original): A memory cell in accordance with claim 3, wherein said variable resistor has a resistance body of a perovskite structure.

Claim 7 (original): A memory cell in accordance with claim 4, wherein said variable resistor has a resistance body of a perovskite structure.

Claim 8 (original): A memory device formed of a plurality of memory cells arranged in a matrix, comprising:

said memory cells, each comprising a variable resistor and a field-effect transistor for controlling a current flowing through said variable resistor;

word lines for connecting the gates of said field-effect transistors in common in the row direction of said matrix;

source drive lines for connecting the sources of said field-effect transistors in common in said row direction; and

bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein

the drains of said field-effect transistors are connected to the other terminals of said variable

resistors.

Claim 9 (original): A memory device in accordance with claim 8, wherein said word lines are connected to a row decoder for selecting said word lines,

said bit lines are connected to a column decoder for selecting said bit lines, and

a readout circuit is connected to said column decoder to read memory data from said memory cells.

Claim 10 (original): A memory device formed of a plurality of memory cells arranged in a matrix, comprising:

said memory cells, each comprising a variable resistor and a diode for controlling a current flowing through said variable resistor;

word lines for connecting the anodes of said diodes in common in the row direction of said matrix; and

bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein

the cathodes of said diodes are connected to the other terminals of said variable resistors.

Claim 11 (original): A memory device in accordance with claim 10, wherein said word lines are connected to a row decoder for selecting said word lines,

said bit lines are connected to a column decoder for selecting said bit lines,

a readout circuit is connected to said column decoder to read memory data from said

memory cells.

Claim 12 (original): A memory device formed of a plurality of memory cells arranged in a matrix, comprising:

said memory cells, each comprising a variable resistor and a bipolar transistor for controlling a current flowing through said variable resistor;

a common-connected portion for connecting the collectors of said bipolar transistors in common;

word lines for connecting the bases of said bipolar transistors in common in the row direction of said matrix;

bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein

the emitters of said bipolar transistors are connected to the other terminals of said variable resistors.

Claim 13 (original): A memory device in accordance with claim 12, wherein said word lines are connected to a row decoder for selecting said word lines, said bit lines are connected to a column decoder for selecting said bit lines, and a readout circuit is connected to said column decoder to read memory data from said memory cells.

Claim 14 (original): A memory device in accordance with claim 9, wherein said variable resistor has a resistance body of a perovskite structure.

Claim 15 (original): A memory device in accordance with claim 11, wherein said variable resistor has a resistance body of a perovskite structure.

Claim 16 (original): A memory device in accordance with claim 13, wherein said variable resistor has a resistance body of a perovskite structure.

Claim 17 (new): A memory cell comprising:

a variable resistor; and

a current controlling device for controlling a current flowing through said variable resistor,

wherein said current controlling device is controlled by a bit line, a word line, and a source drive line,

wherein the bit line is coupled to a column address signal unit of a column decoder, the column address signal unit comprises

a first transistor having a drain terminal coupled to a first potential line, a gate terminal coupled to a column address signal line, and a source terminal coupled to the bit line, and

a second transistor having a drain terminal coupled to a second potential line, a gate terminal coupled to an inverse of the column address signal line, and a source terminal coupled to the bit line.

Claim 18 (new): A memory device in accordance with claim 17, wherein the column

address signal unit further comprises:

a third transistor having a gate terminal coupled to the inverse of the column address signal line, a drain terminal coupled to a readout circuit, and a source terminal coupled to a third potential line.

Claim 19 (new): A memory device in accordance with claim 18, wherein the readout circuit comprises:

a multiplexer for receiving a signal from the drain terminal of the third transistor; and

a differential amplifier for comparing an output signal of the multiplexer to a reference level signal.